AMENDMENTS TO THE SPECIFICATION

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The described embodiments are based on complementary MOS (CMOS) technology. CMOS integrated circuits having PMOS transistors integrated with NMOS transistors are well known, and a process for fabricating CMOS vertical MOSFETs is described in U.S. Serial No. 09/335,646 filed 6/18/99, now abandoned [290533] entitled, "A CMOS Integrated Circuit Having Vertical Transistors and a Process for Fabricating Same," filed on June 18, 1999, now incorporated by reference. A more general description on the fabrication of vertical transistor MOSFETs (of either the NMOS or PMOS type) is taught in commonly assigned U.S. Patent No. 6,027,975 also incorporated herein by reference. Still another commonly assigned, related application, U.S. Serial No. 09/528,753 filed 03/20/2000, now U.S. Patent No. 6,518,622 [341,190], filed on March 20, 2000, teaches the use of silicides in vertical MOSFETs.